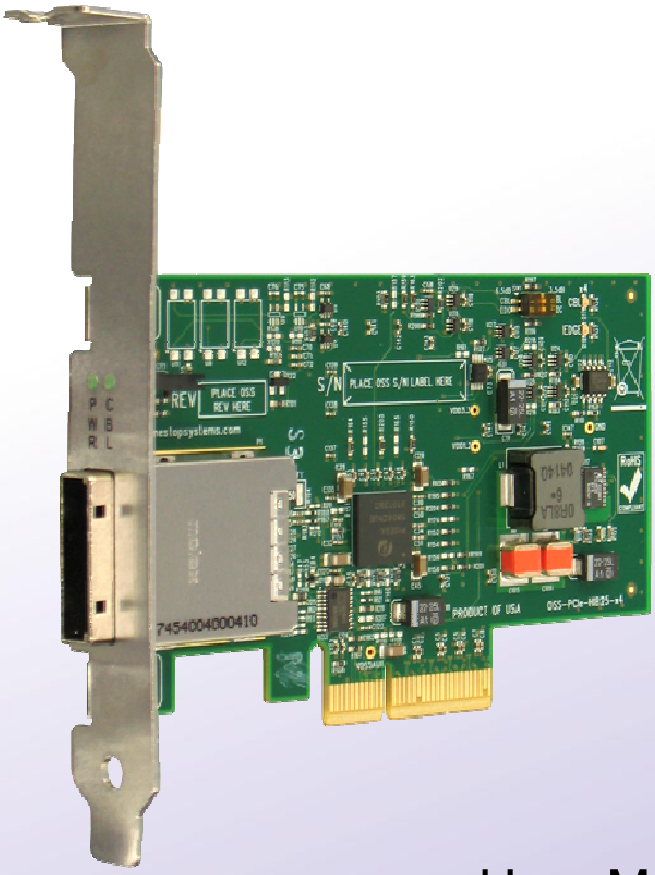
One Stop Systems • 2235 Enterprise Street, Suite #110, Escondido, CA 92029



User Manual,
PCIe x4 Gen 2 Cable Adapter

OSS-PCIe-HIB25-x4-H (Host)
OSS-PCIe-HIB25-x4-T (Target)

MAX EXPRESS™

PCI EXPRESS · CompactPCI Express · PICMG · ISO 9001:2008

www.onestopsystems.com
Phone 877-438-2724 • Fax 760-466-1678 • sales@onestopsystems.com

Table of Contents

1. Overview

1.a. Unpacking instructions 1
1.b. Product description 1
1.c. Specifications 1
1.d. Block diagram 2

2. Initial Setup

2.a. Installation and removal 2
2.b. Installing the host cable adapter 2
2.c. Removing the host cable adapter 4
2.d. When using with any third party I/O device 4

3. Signal adjustments

3.a. Signal adjustment 5

4. Ordering Information

Appendix

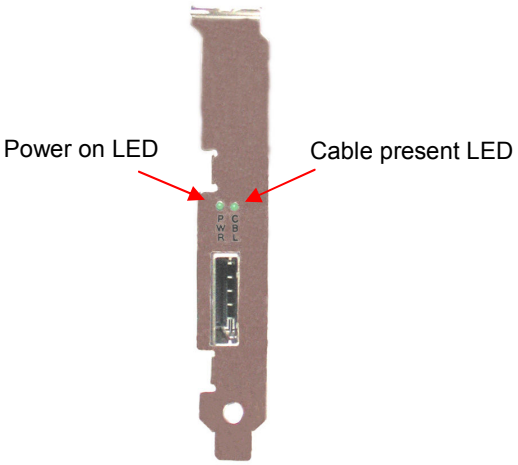
1. Overview

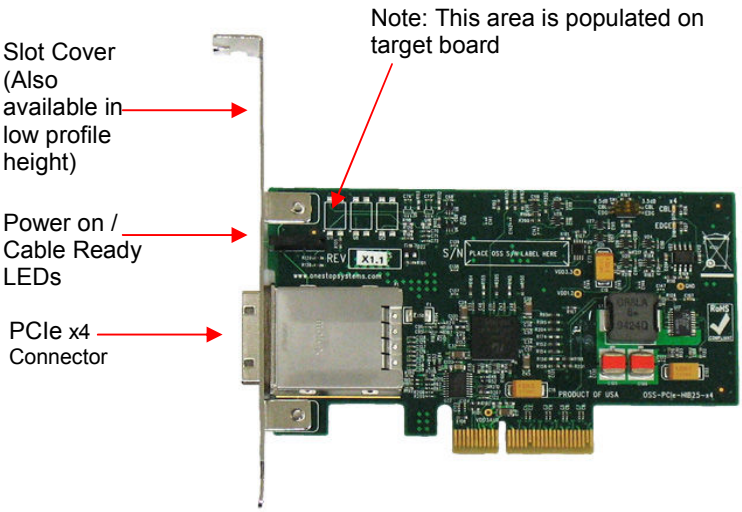
1.a. Unpacking Instructions

1) If the carton is damaged when you receive it, request that the carrier's agent be present when you unpack and inspect the equipment.
2) After unpacking, verify that all items listed in the packing list are present.
3) Inspect the equipment for shipping damage.

1.b. Product Description

The PCIe x4 Gen 2 cable adapter is a PCIe half-height add-in card with a PCIe x4 cable connector on the slot cover. The host cable adapter installs in the PCIe slot of a host server and the target cable adapter installs in the target slot of the OSS 2-slot backplane. Both are sold separately or together with the 2-slot backplane in a kit (OSS-KIT-EXP-3000-2M)

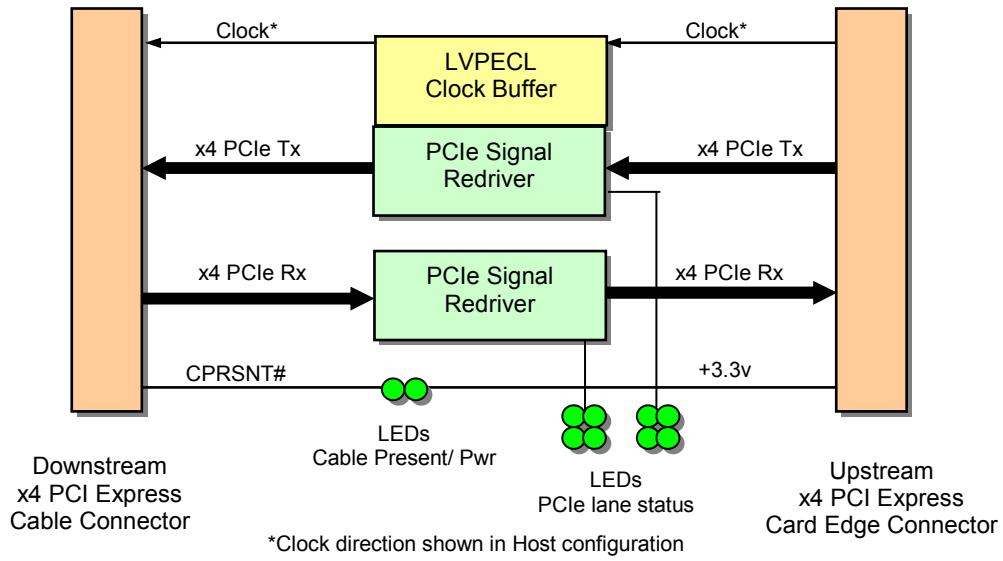



Slot Cover (Also available in low profile height)
Note: This area is populated on target board
Power on / Cable Ready LEDs
PCIe x4 Connector

1.c. Specifications

Dimensions (H x L): 2.7 x 3.1 inches (68 x 78mm)
Front Panel Connectors: One PCIe x4 cable connector
Front Panel Indicators:
Power On / Cable Present: LEDs
Power Consumption (designed to meet the following conditions): 3.75W typical, 3.3@1.3A
Operating Environment (designed to meet the following conditions)
Temperature Range: 0° to 50°C (32° to 122°F)
Relative Humidity: 10 to 90% non-condensing
Shock: 30g acceleration peak (11ms pulse)
Vibration: 5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Redriver: Pericom PI2EQX5804
Agency Compliance: UL60950.FCC Class B, CE

1.d. Block Diagram



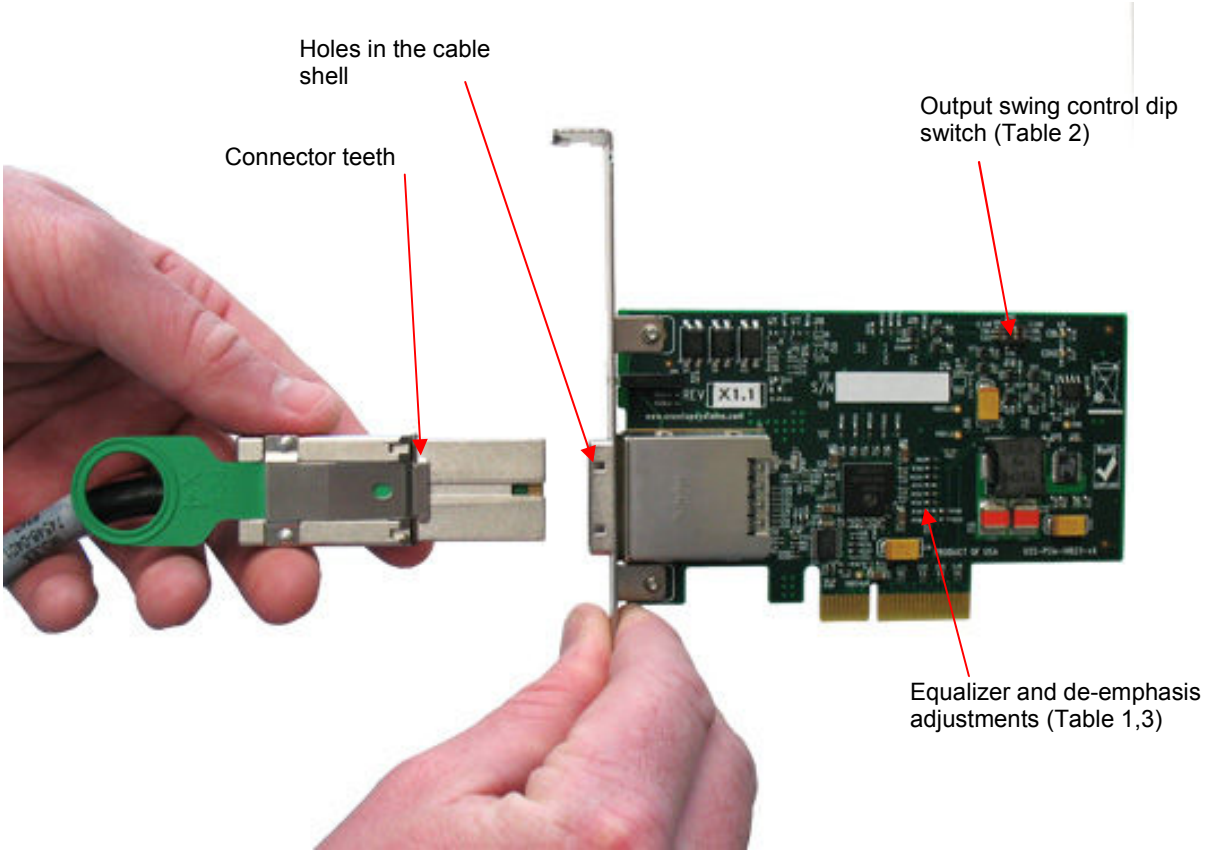
2. Initial Set-Up

2.a. Installation and removal

1) Power down the host system.
2) Open the chassis according to your system documentation.
3) Remove the host cable adapter from the protective bag, observing proper ESD safety procedures.

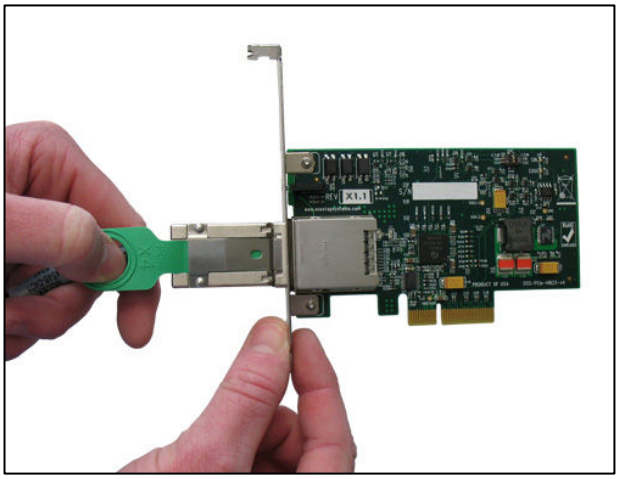
2.b. Installing the host cable adapter:

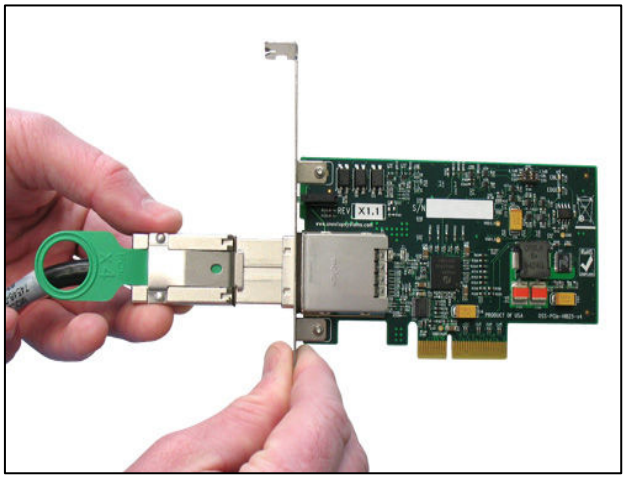
1) Insert the host cable adapter into a PCIe x4, x8 or x16 add-in slot in the host motherboard. Make sure that the card is well seated and tighten the screw on the top of the slot cover.
2) Attach the cable by first pulling back on the retractor ring. Align the keyed slot with the connector key ridge on the slot cover. Insert the cable connector into the connector shell on the board **until the connector teeth snap securely into the holes in the cable shell.**
3) The connectors on either end of the PCIe x4 cable are identical. Each connector is equipped with a retractor to allow the connector to be locked into place.


Holes in the cable shell
Output swing control dip switch (Table 2)
Connector teeth
Equalizer and de-emphasis adjustments (Table 1,3)

2.c. Removing the Host Cable Adapter

1) To remove cable pull back on green thumb tab to release connector teeth and gently separate.





2) Loosen and remove the screw before removing the Host Cable Adapter from the card slot.

2.d. When using with any third party I/O device:

1) Install the downstream board into the appropriate PCIe slot.
2) Connect the external power source (separate from the host system power supply) to the downstream device if necessary.
3) Connect the PCIe cable to both the upstream host adapter and the downstream device.

3. Signal adjustment

3.a. Signal Adjustment

The following chart indicates the default settings for the signal equalization.

SEL_2[A:D]	SEL_1[A:D]	SEL_0[A:D]	@1.25GHZ	@2.5GHZ	
0	0	0	0.5dB	1.2dB	Edge Default
0	0	1	0.6dB	1.5dB	
0	1	0	1.0dB	2.6dB	
0	1	1	1.9dB	4.3dB	
1	0	0	2.8dB	5.8dB	Cable Default
1	0	1	3.6dB	7.1dB	
1	1	0	5.0dB	9.0dB	
1	1	1	7.7dB	12.3dB	

Table 1: Equalizer Selection (refer to call-out on photo)

The following chart indicates the default settings of the –position dip switch for output swing control.

S_1[A:D]	S_0[A:D]	Swing (Diff. VPP)	
0	0	1V	Cable Default
0	1	05V	
1	0	0.7V	Edge Default
1	1	0.9V	

Table 2: Output Swing Control (refer to call-out on photo)

The following chart indicates the default setting for de-emphasis adjustment.

D2_[A:D]	D1_[A:D]	D0_[A;D]	De-emphasis	
0	0	0	0dB	SW=ON Default
0	0	1	-2.5dB	
0	1	0	-3.5dB	
0	1	1	-4.5dB	
1	0	0	-5.5dB	
1	0	1	-6.5dB	SW=OFF Default
1	1	0	-7.5dB	
1	1	1	-8.5dB	

Table 3: De-emphasis Adjustment (refer to call-out on photo)

4. Ordering Information

OSS-PCIe-HIB25-x4-H - One Stop Systems HIB25 x4 host cable adapter.
OSS-PCIe-HIB25-x4-T - One Stop Systems HIB 25 x4 target cable adapter.

Other products you may need;

OSS-PCIe-HIB25-x4-H – PCIe x4 Gen 2 host cable adapter installs in a x4, x8, x16 expansion slot of a host system to extend the host PCIe bus to an expansion system or PCIe device.

OSS-PCIe-HIB25-x4-T – PCIe x4 Gen 2 target cable is only used with the OSS 2-slot PCIe backplane to add a single PCIe card to a host.

OSS-PCIe-HIB25-x8-H – PCIe x8 Gen 2 host cable adapter installs in a x8 or x16 expansion slot of a host system to extend the host PCIe bus to an expansion system or PCIe device.

OSS-PCIe-HIB25-x8-T – PCIe x8 Gen 2 target cable adapter is only used with the OSS 2-slot PCIe backplane to add a single PCIe card to a host.

OSS-PCIe-HIB25-x16-H – PCIe x16 Gen 2 host cable adapter installs in a x16 expansion slot of a host system to extend the host PCIe bus to an expansion system or PCIe device.

OSS-PCIe-HIB25-x16-T – PCIe x16 Gen 2 target cable adapter is only used with the OSS 2-slot PCIe backplane (OSS-PCIeBP-2010, P.34) to add an additional PCIe slot to any device.

OSS-XMC-HIB25-x8 – XMC PCIe x8 Gen 2 host cable adapter installs in an XMC connector on a host carrier board and cables to a PCIe downstream device or expansion chassis.

OSS-PCIe-HIB35-x4 – PCIe x4 Gen 2 cable adapter with PCIe switch (including NT port and DMA controller) operates in upstream or downstream mode with DIP switch setting change.

OSS-SHB-ELB-x4/x8-2.0 – PCIe x8 or x4 Gen 2 expansion link board installs in SHBe slot of a PCIe Gen 2 backplane, allowing either x8 or x4 cable inputs from upstream host system.

OSS-PCIe-CA-x1/x4 – PCIe cable adapter fits into slot or stand-alone, converts PCIex1 cable to PCIex4 cable.

OSS-PCIe-CA-x4/x8 – PCIe cable adapter fits into slot or stand alone, converts PCIex4 cable to PCIe x8 cable.

OSS-PCIe-CBL-x4-1M – 1 meter PCIe x4 cable with PCIe x4 connectors.

OSS-PCIe-CBL-x4-2M – 2 meter PCIe x4 cable with PCIe x4 connectors.

OSS-PCIe-CBL-x4-3M – 3 meter PCIe x4 cable with PCIe x4 connectors.

OSS-PCIe-CBL-x4-5M – 5 meter PCIe x4 cable with PCIe x4 connectors.

OSS-PCIe-CBL-x4-7M – 7 meter PCIe x4 cable with PCIe x4 connectors.

OSS-PCIe-CBL-ACT-x4-10M – 10 meter active optical cable with PCIe x4 connectors.

OSS-PCIe-CBL-ACT-x4-100M – 100 meter active optical cable with PCIe x4 connectors.

Appendix

Pin Assignments

Connectors PCIe x4 Card Edge Connector

- The pins are numbered as shown with side A on the top of the centerline on the solder side of the board and side B on the bottom of the centerline on the component side of the board.
- The PCIe interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCIe high speed, “T” for Transmitter, “R” for Receiver, “p” for positive (+), and “n” for negative (-).
- Note that adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.

Pin #	Side B		Side A	
	Name	**Description**	**Name**	**Description**
1	N/C	N/C	PRSNT1#	Hot-Plug presence detect
2	N/C	N/C	N/C	N/C
3	N/C	N/C	N/C	N/C
4	GND	Ground	GND	Ground
5	NC	N/C	N/C	Not connected
6	N/C	N/C	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3 V power	N/C	Not connected
9	N/C	Not connected	N/C	Not connected
10	3.3Vaux	3.3 V auxiliary power	+3.3V	3.3 V power
11	N/C	N/C	PERST#	Fundamental reset
Mechanical key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair, Lane 1	RSVD	Reserved
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2

26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	RSVD	Reserved	PERn3	
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

Table 1: Pin-out for the PCIe x4 Card Edge Connector on the Host Cable Adapter

Notes:

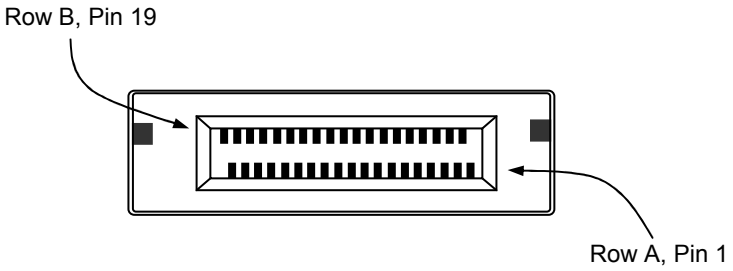
1 Optional signals that are not implemented are to be left as no connects on the board side connector.

2 Reserved signals must be left as no connects on the board side connector.

3 Although support of CWAKE# is optional from the board side connector perspective, an allocated wire is mandated for the cable assembly.

4 Board side pin-out on both sides of the Link is identical. The cable assembly incorporates a null modem for the PCIe transmit and receive pairs.

PCI Express x4 Cable Connector Pin out



Pin #	Cable Side 1		Cable Side 2	Pin #
A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13	GND	Drain Wires	GND	A1 A4 A7 A10 A13 A16 B1 B4 B7 B10 B13
A2	PETp0	Differential Pair	PERp0	B2
A3	PETn0		PERn0	B3
A5	PETp1	Differential Pair	PERp1	B5
A6	PETn1		PERn1	B6

Pin #	Cable Side 1		Cable Side 2	Pin #
A8	PETp2	Differential Pair	PERp2	B8
A9	PETn2		PERn2	B9
A11	PETp3	Differential Pair	PERp3	B11
A12	PETn3		PERn3	B12
A14	CREFCLK+	Differential Pair	CREFCLK+	A14
A15	CREFCLK		CREFCLK-	A15
A17	SB_RTN	Hook-up Wire	SB_RTN	A17
A18	CPRSNT#	Hook-up Wire	CPRSNT#	A18
A19	CPWRON	Hook-up Wire	CPWRON	A19
B2	PERp0	Differential Pair	PETp0	A2
B3	PERn0		PETn0	A3
B5	PERp1	Differential Pair	PETp1	A5
B6	PERn1		PETn1	A6
B8	PERp2	Differential Pair	PETp2	A8
B9	PERn2		PETn2	A9
B11	PERp3	Differential Pair	PETp3	A11
B12	PERn3		PETn3	A12
B14	PWR	NC	PWR	B14
B15	PWR	NC	PWR	B15
B16	PWR_RTN	NC	PWR_RTN	B16
B17	PWR_RTN	NC	PWR_RTN	B17
B18	CWAKE#	Hook-up Wire	CWAKE#	B18
B19	CPERST#	Hook-up Wire	CPERST#	B19
Back shell	Chassis Ground	Overall Cable Braid	Chassis Ground	Back shell

PIN- out for the PCIe x4 Cable

Signal Descriptions

PETp(x)	PCI Express Transmit Positive signal of (x) pair.
PETn(x)	PCI Express Transmit Negative signal of (x) pair.
PERp(x)	PCI Express Receive Positive signal of (x) pair.
PERn(x)	PCI Express Receive Negative signal of (x) pair.
CREFCLK+/-	Cable REFerence CLocK: Provides a reference clock from the host system to the remote system.
SB_RTN	Side Band ReTurN: return path for single ended signals from remote systems.
CPRSNT#	Cable PReSeNT: Indicates the presence of a device beyond the cable.
PWR	PoWeR: Provides local power for in-cable redriver circuits. Only needed on long cables. Power does not go across the cable.)
PWR_RTN	PoWeR ReTurN: Provides local power return path for PWR pins.
CWAKE#	Cable WAKE
CPERST#	Cable PCI Express Reset